Dawud Benedict

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Driven Computer Engineering student specializing in digital VLSI design and verification. Strong background in RTL design and microarchitecture, with experience in FPGA prototyping and simulation. Seeking a Summer 2026 internship to apply skills in ASIC design and functional verification.

Education:

Iowa State University – Ames, IA **Expected May 2026**
Bachelor of Science in Computer Engineering – GPA: 4.0/4.0

Des Moines Area Community College – Ankeny, IA **Graduated May 2023**
Associate of Science in Pre-Engineering – GPA: 3.9/4.0

Skills:

- **Programming:** C/C++, Java, Assembly, Python, MATLAB, Bash.
- **Hardware Design:** Verilog, VHDL, RTL design, FPGA prototyping, CPU design, timing analysis.
- **Software:** QuestaSim, Git, Cadence Virtuoso, MySQL, Linux.

Employment:

Research Assistant – Ames, IA **May 2025 – Present**
Iowa State University

- Investigating hardware prefetcher architectures to increase memory performance and reduce processor stalls.
- Analyzing prefetcher timeliness, accuracy, and coverage through FPGA-based simulations.
- Designing and synthesizing RISC-V SoC designs for FPGA prototyping using a Vivado based toolflow.

Digital Logic Teaching Assistant – Ames, IA **January 2024 – June 2024**
Iowa State University

- Led weekly labs and recitations to reinforce digital logic concepts with Verilog projects.
- Collaborated with faculty and TAs to create fair grading rubrics for exams and labs.

General Manager – Des Moines, IA **March 2021 – August 2023**
Hilal Groceries

- Trained new employees to work the cashier, stock, organize products, and handle customer communication.
- Organized the company by implementing inventory management, order tracking, and financial sheets using Excel.

Projects:

Graphics Accelerator – Senior Design Project **August 2025 – May 2026**

- Developing a hardware rasterizer / 3D graphics adapter with custom VGA output.
- Implementing digital VLSI flow: RTL development, functional verification, synthesis, and FPGA prototyping.
- Architecting a memory system with external RAM interfaces and internal caching for textures and frame buffers.

MIPS 5-stage Pipeline Processor **February 2025 – May 2025**

- Designed and verified single-cycle and 5-stage pipelined MIPS processors in VHDL.
- Implemented hazard detection, forwarding, and branch control to improve performance.
- Built testbenches for verification and synthesized processors to evaluate timing, critical paths, and compare performance trade-offs.

4B5B Serial Communication Chip Design **October 2024 – December 2024**

- Designed a Verilog serial encoder converting 4-bit parallel data into a 5-bit serial stream.
- Verified functionality with self-checking Verilog testbenches and waveform debugging in QuestaSim.
- Synthesized RTL to gate-level schematics and validated with DRC/LVS checks.