Dawud Benedict

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Seeking a digital design internship to apply knowledge in FPGA/ASIC design, RTL development, and hardware verification, while gaining hands-on industry experience.

Education:

Iowa State University – Ames, IA **Expected May 2026**
Bachelor of Science in Computer Engineering – GPA: 4.0/4.0

Des Moines Area Community College – Ankeny, IA **Graduated May 2023**
Associate of Science in Pre-Engineering – GPA: 3.9/4.0

Skills:

- **Programming:** C/C++, Java, Assembly, Python, MATLAB.
- **Software:** Git, QuestaSim, Cadence Virtuoso, MySQL, Linux Command Line, Windows, MacOS.
- **Hardware Design:** Verilog, VHDL, RTL design, FPGA synthesis (Xilinx Vivado), CPU design, timing analysis.

Employment:

Research Assistant – Ames, IA **May 2025 – Present**
Iowa State University

- Researching hardware prefetchers designs to increase memory performance and reduce processor stalls.
- Analyzing prefetcher implementations to improve prefetch timeliness, accuracy, and coverage.
- Generate and synthesize RISC-V SoC designs for FPGA deployment using a Vivado-based tool flows.

Digital Logic Teaching Assistant – Ames, IA **January 2024 – June 2024**
Iowa State University

- Led weekly lab sessions with recitations, and provided office hours to improve students' understanding.
- Collaborated with other teaching assistants to create fair grading rubrics for exams and labs.

General Manager – Des Moines, IA **March 2021 – August 2023**
Hilal Groceries

- Trained new employees to work the cashier, stock and organize products, and communicate with customers.
- Utilized Excel to create and maintain order sheets and track inventory, helping company organization.

Projects:

MIPS 5-stage Pipeline Processor **February 2025 – May 2025**

- Designed and verified both single stage and 5-stage pipelined MIPS processors in VHDL.
- Included hazard avoidance and forwarding to minimize CPI.
- Created simulation testbenches to verify functional correctness and
- Synthesized the processors to evaluate timing, critical paths, and compare performances.

Embedded Autonomous Warehouse Robot **October 2024 – December 2024**

- Programmed a Tiva TM4C123GH6PM microcontroller to control iRobot Create 2 for autonomous warehouse navigation.
- Configured the Tiva's PWM, GPIO, ADC, and UART interfaces for sensor integration and iRobot control.
- Implemented a Python-based GUI for real-time robot location tracking, sensor reading, and obstacle visualization.

4B5B Serial Communication Chip Design **October 2024 – December 2024**

- Designed a Verilog serial communication chip to encode a 4-bit parallel input into 5-bit serial data.
- Implemented components, including a shift register, counter, clock divider, and encoder, simulated within Questa.
- Synthesized RTL design into hardware schematics used for physical layout.